

REMARKS

The Office Action dated June 20, 2006 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto. Claim 1 has been amended to correct a formality, however, no new matter has been introduced. Therefore, claims 1-23 are pending and submitted for consideration herein.

Claims 1, 18, and 23 stand rejected under 35 U.S.C. §102(a) as being anticipated by *Sadjadpour* (U.S. Publication No. 2001/0055332). The Office Action took the position that *Sadjadpour* teaches each and every element recited in the rejected claims. Applicants traverse the rejection and respectfully submit that each of claims 1, 18, and 23 recite subject matter that is not taught or disclosed by *Sadjadpour*.

Independent claim 1, upon which claims 2-4, 9, and 11-14 depend, recites a communication system for transferring data between a transmitter and a receiver over a plurality of channels. The communication system includes modulation circuitry having a plurality of modulation alphabets providing a set of a bit loading sequences. The system further includes circuitry for determining a power allocation for at least one bit loading sequence based on minimizing an error rate, and circuitry for selecting a bit loading sequence with a lowest error rate.

Independent claim 18 recites a method for transferring data between a transmitter and receiver over a communication channel. The method includes identifying a set of bit loading sequences from a plurality of modulation alphabets, determining a power

allocation for at least one bit loading sequence based on minimizing an error rate, and selecting a bit loading sequence with a lowest error rate and applying the power allocation to at least one communication channel.

Independent claim 23 recites a communication system for transferring data between a transmitter and a receiver over a plurality of channels. The communication system includes a providing means for providing a modulation circuitry having a plurality of modulation alphabets and for providing a set of a bit loading sequences. The system further includes a determining means for determining a power allocation for at least one bit loading sequence based on minimizing an error rate, and selecting means for selecting a bit loading sequence with a lowest error rate.

Applicants submit that *Sadjadpour* fails to teach or disclose each and every element recited in rejected claims 1, 18, and 23. More particularly, *Sadjadpour* teaches a discrete multi-tone modem that operates to minimize cross talk over a twisted pair cable. The spectrum of the twisted pair cable can be split into multiple sub-bands or QAM channels, where each channel is able to handle K_i bits of data, where i is the member of the channel, as described in paragraph [0027]. The bit addition algorithm of *Sadjadpour* describes how an array of different bit allocation settings are ordered in ascending order so that bit allocation can be determined based on the least possible power for the maximum data rate possible or a desired data rate, as described in paragraphs [0037]-[0038]. Bits are then added and the process continued until the addition of any further bit in any of the frequency bins violates at least one predetermined constraint, such as power

budget, power mask, or maximum number of bits per frame, for example. Further, in another described embodiment of *Sadjadpour*, the method of allocating bits is modified by modifying the incremental power term by a weighting dependent on the frequency of the tone (sub-frequency). The effect of this weighting function forces the algorithm towards the lower frequencies, which according to the disclosure, has the effect or goal of reducing the near end cross talk (NEXT) power.

However, Applicants submit that *Sadjadpour* does not teach or suggest circuitry configured to select a bit loading sequence with a lowest error rate, as recited in claim 1. Similarly, *Sadjadpour* also does not teach or disclose a selecting means for selecting a bit loading sequence with a lowest error rate, as recited in claim 23. Further, *Sadjadpour* does not teach or disclose determining a power allocation for at least one bit loading sequence based on minimizing an error rate, as recited in claim 18.

More particularly, with regard to claims 1 and 23, the Examiner has indicated that *Sadjadpour* discloses the circuitry recited in claims 1 and 23 in paragraphs [0043]-[0046]. These paragraphs of *Sadjadpour*, which describe Figure 6, show the various inputs which are required in order to operate the bit allocation algorithm. Thus, blocks 61-68 represent the various objective functions with the shaded blocks of Figure 6 being those used to reduce the cross talk. Therefore, function 64 represents the joint minimization of an arbitrary function of the total power and maximization of the total data rate such as would be achieved using the algorithm described in paragraphs [0036]-[0038]. Similarly, function block 61 shows the functions which apply joint minimization

of the cross talk and maximization of the total data rate, as is shown in the method described in paragraphs [0039]-[0042].

Therefore although *Sadjadpour* does disclose selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk, there is no disclosure of circuitry for selecting a bit loading sequence with the lowest error rate. As such, Applicants submit that *Sadjadpour* fails to teach or disclose each and every element recited in claims 1 and 23, and therefore, reconsideration and withdrawal of the rejection of claims 1 and 23 over *Sadjadpour* is respectfully requested.

With regard to the method recited in claim 18, Applicants submit that *Sadjadpour* fails to teach the recited limitation of determining a power allocation for a bit loading sequence based on minimizing an error rate. As noted above, *Sadjadpour* does not teach or disclose power allocation for bit loading frequencies based on minimizing the error rate; rather, *Sadjadpour* discloses only power allocation based only on reducing the cross talk. There is no teaching or suggestion in *Sadjadpour* of power allocation for bit loading frequencies based on minimizing the error rate, and as such, Applicants submit that it is incorrect for the Office Action to suggest or conclude, without specific citation to the prior art, that *Sadjadpour* teaches power allocation for bit loading frequencies based on minimizing the error rate when only cross talk is discussed in *Sadjadpour*. Therefore, although *Sadjadpour* discloses determining a power allocation for at least one bit loading sequence, *Sadjadpour* does not do so for a sequence based on minimizing an error rate, as

recited in claim 18. As such, reconsideration and withdrawal of the rejection of claim 18 over *Sadjadpour* is respectfully requested.

Claims 2-13, 19, 20, and 22 stand rejected under 35 U.S.C. §103(a) as being obvious in view of *Sadjadpour* in view of Applicants' admitted prior art (Fig. 1-2 and [0005]-[0023], hereafter, AAPA). The Office Action took the position that *Sadjadpour* teaches each and every element recited in claims 2-13, 19, 20, and 22, except for the MIMO system. However, the Office Action cites to AAPA as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the cited prior art to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claims 2-13, 19, 20, and 22.

Applicants' independent claim 1 is presented above. Applicants' independent claim 19 recites a communication system for transferring data between a transmitter and receiver over a communication channel. The system includes a first circuitry means for decomposing a communication channel into a plurality of logical channels, and a modulation circuitry having a plurality of modulation alphabets, at least two modulation alphabets are capable of representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels. The circuitry also includes a second circuitry means for allocating a power weighting to the corresponding logical channels

for minimizing a bit error rate of the identified bit loading sequences, and a third circuitry for choosing a bit loading sequence having a minimum bit error rate.

Applicants' independent claim 20, upon which claim 21 depends, recites a method for transferring data between a transmitter and receiver over a communication channel. The method includes decomposing a communication channel into a plurality of logical channels, and selecting from a plurality of modulation alphabets, wherein at least two modulation alphabets for modulating data are capable of representing the data using a different number of bits. The method further includes identifying a set of bit loading sequences for a fixed data rate which specify a number of bits to be loaded onto corresponding logical channels of the plurality of channels, allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences, and choosing a bit loading sequence having a minimum bit error rate.

Applicants' independent claim 22 recites a communication system for transferring data between a transmitter and receiver over a communication channel. The system includes a decomposing means for decomposing a communication channel into a plurality of logical channels, and a representing means for representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels. The system further includes an allocating means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the

identified bit loading sequences, and a choosing means for choosing a bit loading sequence having a minimum bit error rate.

Applicants' submit that each of claims 2-13, 19-20, and 22 recite subject matter that is not taught, shown, or suggested by the cited combination of prior art references. More particularly, *Sadjadpour* is discussed above and AAPA can be found at paragraphs [0005]-[0023] of Applicants' specification.

However, as noted above, *Sadjadpour* does not teach or disclose circuitry configured to select a bit loading sequence with a lowest error rate, as recited in each of claims 2-13. Similarly, as noted above, *Sadjadpour* does not teach or disclose a third circuitry or choosing means for choosing a bit loading sequence having a minimum error rate, as recited in each of claims 19 and 22. Further, as noted above, *Sadjadpour* also does not teach or disclose allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based on minimizing an error rate, as recited in claims 20 and 21. Each of these deficiencies is noted above in the discussion of claims 1, 18, and 23.

Further, Applicants submit that the cited portions of Applicants' specification (paragraphs [0005]-[0023]) also do not teach, show, or suggest the limitation recited in claims 2-13, 19-20, and 22. More particularly, Applicants submit that AAPA does not teach the circuitry configured to select a bit loading sequence with a lowest error rate, or allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based

on minimizing an error rate. As such, Applicants submit that AAPA does not further the teaching of *Sadjadpour* to the level necessary to properly support an obviousness rejection of claims 2-13, 19-20, and 22. Therefore, reconsideration and withdrawal of the rejection of these claims is respectfully requested.

Claims 14-17 and 21 stand rejected under 35 U.S.C. §103(a) as being obvious in view of *Sadjadpour* in view of AAPA, further in view of *Kim* (U.S. Publication No. 2003/0128769). The Office Action took the position that *Sadjadpour* teaches each and every element recited in claims 14-17 and 21, except for codings and modulations that utilize system bits. However, the Office Action cites to *Kim* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claims 14-17 and 21.

Applicants' independent claims 1 and 20, the independent claims from which claims 14-17 and 21 depend, are presented above. Similarly, *Sadjadpour* and AAPA are discussed above. *Kim* generally teaches a method for providing first and second interleaved bit streams to a modulator in order to transmit the first and second interleaved bit streams through at least two antennas in a mobile communication system. An encoder encodes a transmission data stream into a first bit stream with first priority and a second bit stream with second priority being lower than the first priority. An interleaver

interleaves the first and second bit streams into the first and second interleaved bit streams. The modulator modulates the first and second interleaved bit streams.

However, *Kim* does not teach, show, or suggest circuitry configured to select a bit loading sequence with a lowest error rate, as recited in each of claims 14-17. Similarly, *Kim* does not teach or disclose allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based on minimizing an error rate, as recited in claims 20 and 21. Since these limitations are also not taught or disclosed by *Sadjadpour* or *AAPA*, as discussed above, Applicants submit that *Kim* fails to further the teaching of *Sadjadpour* and *AAPA* to the level necessary to properly support an obviousness rejection. As such, reconsideration and withdrawal of the rejection of claims 14-17 and 21 is respectfully requested.

With regard to each of the obviousness rejections discussed above, Applicants submit that in addition to the above noted remarks, Applicants further note that the method shown in the description of *Sadjadpour* is specifically related to the problem of cross talk in twisted pair modems, and as such, the method of *Sadjadpour* describes a weighting algorithm to reduce cross talk based on twisted pair cross talk algorithms. Applicants note that even if a person of skill in the art were to examine the teaching of *Sadjadpour*, they would not have considered *Sadjadpour* to be a suitable starting point for generating Applicants' claimed invention, as fields of wired and wireless communication are significantly different in most aspects. Applicants submit that one of

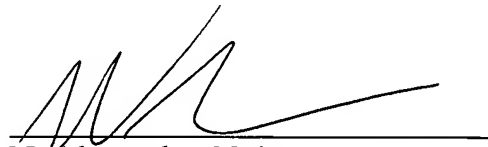
skill in the art working in a twisted pair environment would not look to a wireless solution to solve a twisted pair problem. Thus Applicants submit that in the absence of any teaching, suggestion, or motivation to do so found in the references themselves, a person skilled in the art would not have considered modifying a twisted pair modem communication technique for application in a wireless communication system, and combination of such teachings is inappropriate. Thus, Applicants submit that the references cited in support of the §103 rejection are not properly combined, and reconsideration and withdrawal of the obviousness rejections is respectfully requested.

In conclusion, Applicants submit that each of claims 1-23 recites subject matter that is not taught, disclosed, or otherwise suggested by the cited prior art, when taken alone or in combination. Therefore, reconsideration and withdrawal of the rejections of claims 1-23 is respectfully requested.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'N. Alexander Nolte', is written over a horizontal line.

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Enclosures: Petition for Extension of Time
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